CHENMKO ENTERPRISE CO.,LTD

Halogens free devices

SURFACE MOUNT

CHM3U22VESGP

Dual Enhancement Mode Field Effect Transistor

N-channel: VOLTAGE 30 Volts CURRENT 0.2 Ampere
P-channel: VOLTAGE 30 Volts CURRENT 0.2 Ampere

APPLICATION

* High speed switching , Analog switching

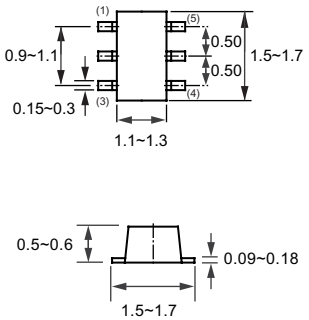
FEATURE

* Small flat package. (SOT-563)
* Super high dense cell design for extremely low $R_{DS(ON)}$.
* Lead free product is acquired.
* High power and current handing capability.
* ESD protect in input gate 2KV

CONSTRUCTION

* N-Channel & P-Channel Enhancement in the package

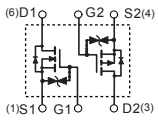
SOT-563



Dimensions in millimeters

SOT-563

CIRCUIT



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	±8	±8	V
I_D	Maximum Drain Current - Continuous	200	-200	mA
	- Pulsed (Note 3)	400	-400	
P_D	Maximum Power Dissipation	125		mW
T_J	Operating Temperature Range	-55 to 150		°C
T_{STG}	Storage Temperature Range	-55 to 150		°C

Note : 1. Surface Mounted on FR4 Board , t <=10sec
2. Pulse Test , Pulse width <= 300us , Duty Cycle <= 2%
3. Repetitive Rating , Pulse width linited by maximum junction temperature
4. Guaranteed by design , not subject to production trsting

ELECTRICAL CHARACTERISTIC (CHM3U22VESGP)

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

SYMBOL	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D=100μA, V_{GS}=0V	30	–	–	V
I_{GSS}	Gate-source leak current	V_{GS}=±5V, V_{DS}=0V	–	–	±0.5	μA
I_{DSS}	Zero gate voltage drain current	V_{DS}=30V, V_{GS}=0V	–	–	1.0	μA
V_{th}	Gate threshold voltage	I_D=250μA, V_{DS}=V_{GS}	0.6	–	1.2	V
$\lvert Y_{fs} \rvert$	Forward transfer admittance	V_{DS}=10V, I_D=0.1A	–	300	–	mS
$R_{DS(ON)}$	Static drain-source on-state resistance	I_D=100mA, V_{GS}=4.0V	–	1.1	–	Ω
C_{iss}	Input capacitance	V_{DS}=10V, V_{GS}=0V, f=1MHz	–	33	–	pF
C_{oss}	Output capacitance		–	6.8	–	
t_{on}	Switching time	V_{DD}=5V, I_D=10mA V_{GS}=0～5V	–	12	–	ns
t_{off}			–	80	–	

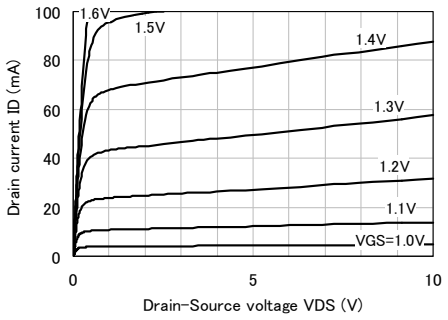
P-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

SYMBOL	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D=−100μA, V_{GS}=0V	−30	–	–	V
I_{GSS}	Gate-source leak current	V_{GS}=±5V, V_{DS}=0V	–	–	±0.5	μA
I_{DSS}	Zero gate voltage drain current	V_{DS}=−30V, V_{GS}=0V	–	–	−1.0	μA
V_{th}	Gate threshold voltage	I_D=−250μA, V_{DS}=V_{GS}	−0.6	–	−1.2	V
$\lvert Y_{fs} \rvert$	Forward transfer admittance	V_{DS}=−10V, I_D=−0.1A	–	220	–	mS
$R_{DS(ON)}$	Static drain-source on-state resistance	I_D=−100mA, V_{GS}=−4.0V	–	3.0	–	Ω
C_{iss}	Input capacitance	V_{DS}=−10V, V_{GS}=0V, f=1MHz	–	35	–	pF
C_{oss}	Output capacitance		–	7.3	–	
t_{on}	Switching time	V_{DD}=−5V, I_D=−10mA V_{GS}=0～−5V	–	14	–	ns
t_{off}			–	100	–	

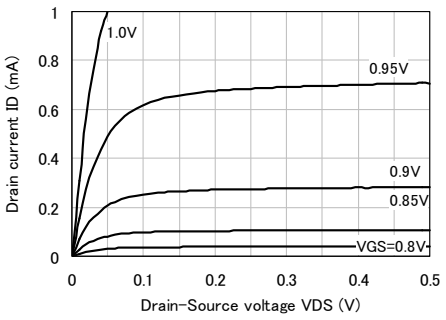
RATING CHARACTERISTIC CURVES (CHM3U22VESGP)

N-MOSFET Typical Electrical Characteristics

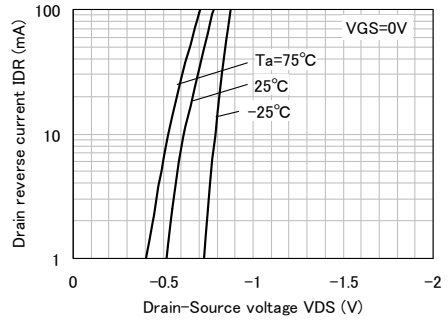
Ta=25°C ID – VDS



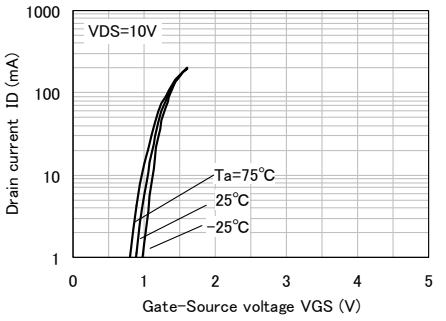
Ta=25°C ID – VDS(Low voltage region)



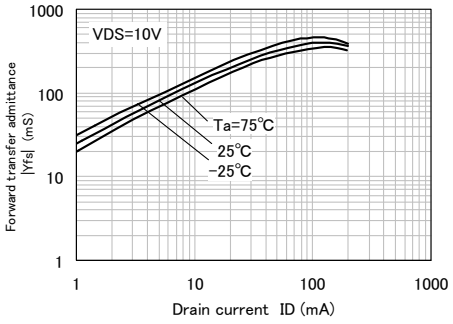
IDR – VDS



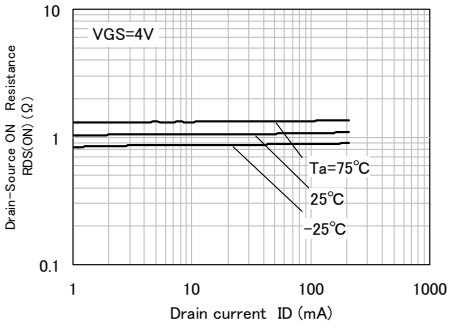
ID – VGS



|Yfs| – ID



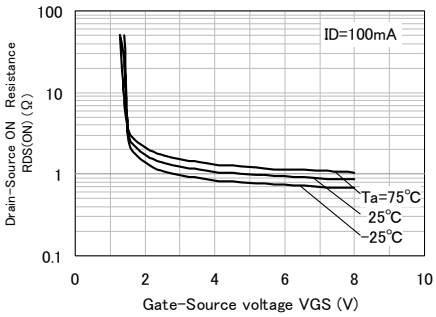
RDS(ON) – ID



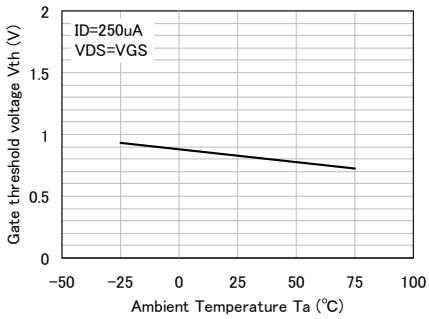
RATING CHARACTERISTIC CURVES (CHM3U22VESGP)

N-MOSFET Typical Electrical Characteristics

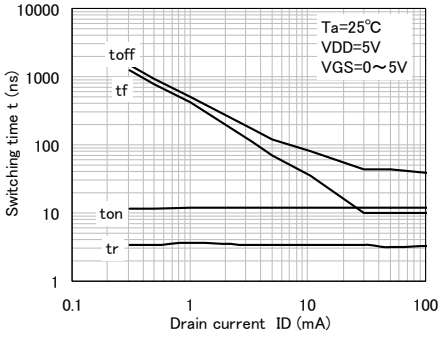
RDS(ON) – VGS



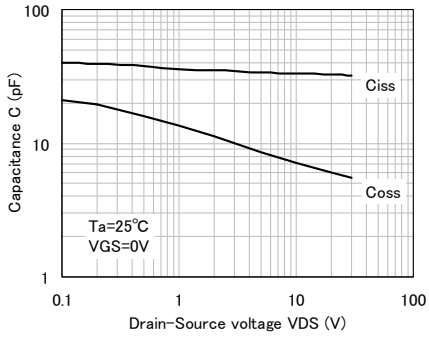
Vth – Ta



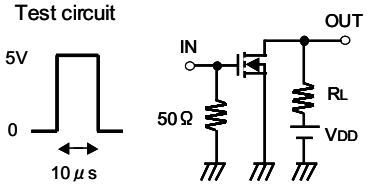
t – ID



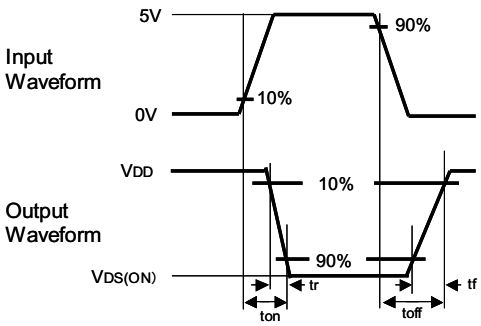
C – VDS



Test circuit

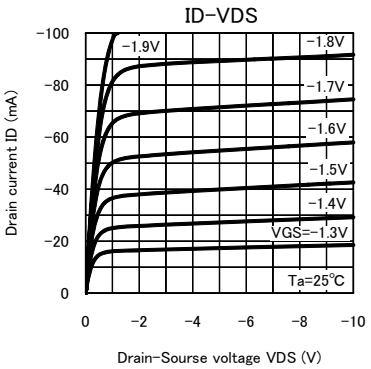


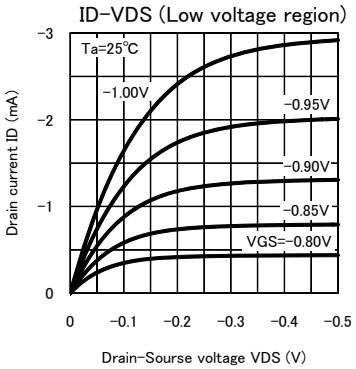
VDD=5V
Duty≦1%
Common source
Ta=25℃

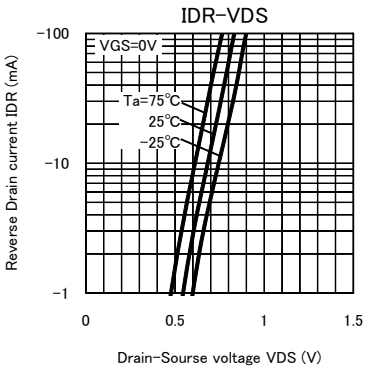


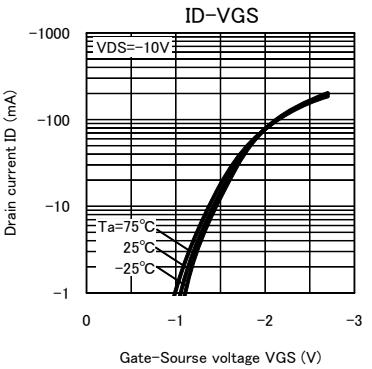
RATING CHARACTERISTIC CURVES (CHM3U22VESGP)

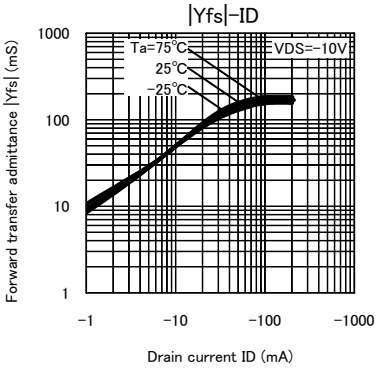
P-MOSFET Typical Electrical Characteristics

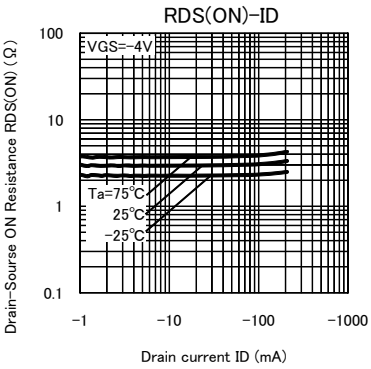






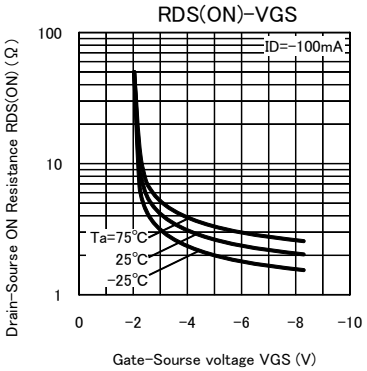


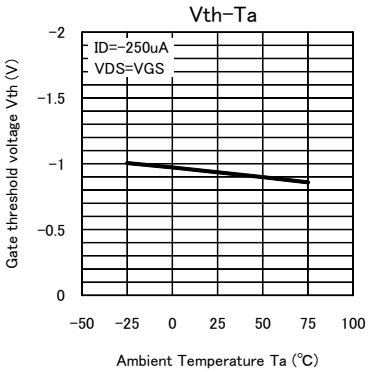


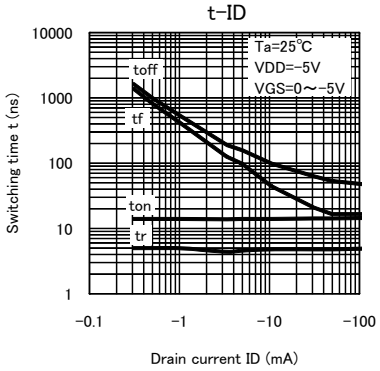


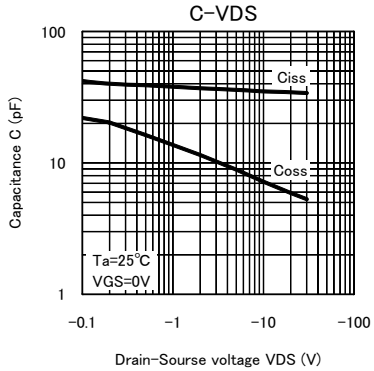
RATING CHARACTERISTIC CURVES (CHM3U22VESGP)

P-MOSFET Typical Electrical Characteristics



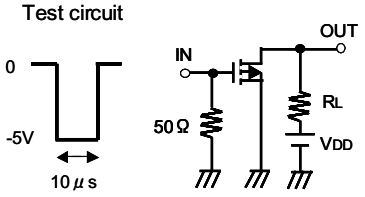






Tr2 Switching time test condition

Test circuit



VDD=-5V
Duty≦1%
Common source
Ta=25℃